REMARKS

Claims 1-30 are pending in the application.

Claims 1-30 have been rejected.

Claims 1, 3, 7, 9, 10, 12, 18, 19, 21, and 26, have been amended to correct minor informalities.

No new matter has been added.

Reconsideration of the Claims is respectfully requested.

1. Claim Objections

The claims were objected to due to informalities. Appropriate correction has been made.

2. Rejection under 35 U.S.C. § 112

Claims 1 - 30 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In general, the rejection is directed towards lack of antecedence within some claims. Appropriate correction has been made.

The rejection also comments on use of the term "substantial" within the claims. Applicant respectfully submits that one of ordinary skill in the art would be reasonably apprised of the scope of Applicant's invention. MPEP § 2173.05(b), p. 2100-215 (Rev. 5, Aug. 2006). The term "substantially" is respectfully submitted as often used in conjunction with another term to describe a particular characteristic of the claimed invention. *Id.* at p. 2100-216.

3. Rejection under Section 102

For establishing anticipation, "[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. . . . The identical invention must be shown in as complete detail as is contained in the . . . claim." MPEP 2131 at p. 2100-67 (Rev. 5, August 2006) (citations omitted).

Claims 21 and 26 were rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,940,456 to Chen et al. ("Chen").

Chen relates to "system that allows multiple bundles of plesiochronous digital hierarchy payload data streams to be synchronously transmitted from one point to another." (Chen 2:39-42). Chen recites multiplexing to avoid stuffing processes at the multiplexing stages. Chen recites that "PDH multiplexing are accomplished in *a single device*, there is no need to perform these stuffing and de-stuffing processing at every stage of the multiplexing. This is because from the first stage (e.g. E1/E2 multiplexing) on, all tributaries can share the same clock source in the system." (Chen 2:).

Though a clock source is shared by all tributaries in Chen, Applicant respectfully submits that a common clock source is not "symmetrically distributing" nor does Chen recite symmetrical clock pathways in which the clock transmission times are substantially equal. As a further example, Chen does not recite the use of a first and a second integrated multiplexing circuit.

Figure 11C of Applicant's Specification depicts a multiplexing circuit utilizing a symmetrical distributed clock:

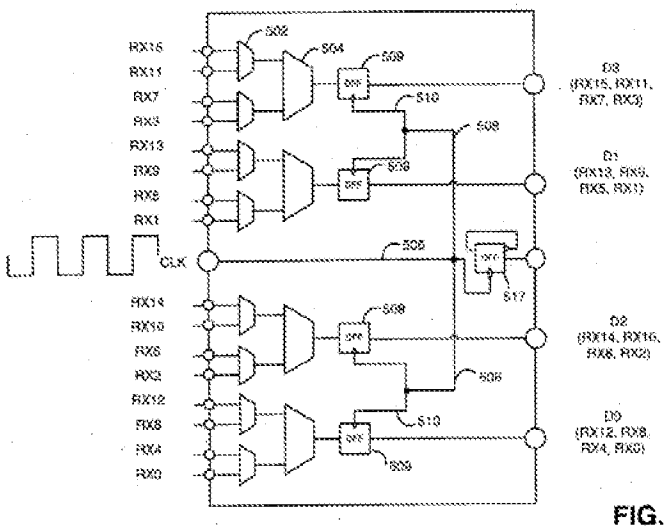

FIG. 11C

In Applicant's Figure 11C, "the clock is distributed from a central trunk 506 to a first set of symmetrical branches 508. The symmetrical branches 508 further divide into symmetrical branches 510 which provide the clock signal to [retimers or] DFFs 509[, which ensure the data is properly aligned in time to the output clock signal]." As explained, "the clock signal is uniformly distributed to DFFs 509 while minimizing skewing. Symmetrical distribution of the clock signal reduces or minimizes skewing by having each clock signal pathways have substantially equal transmission times." (Specification at p. 23, lines 4-11).

Accordingly, Applicant's Independent Claim 21 recites, *inter alia*, a "multistage bit stream multiplexer, comprising: *a first multiplexing integrated circuit* that receives a first plurality of bit streams at a first bit rate and that produces a second plurality of bit streams at a second bit rate, . . . ; a clock circuit, wherein the clock circuit generates a forward data clock signal; *a plurality of symmetrical data circuit pathways* that transport the second plurality of bit streams from the first multiplexing integrated circuit; *a second multiplexing integrated circuit* that receives the second plurality of bit streams from the *plurality of symmetrical data circuit pathways*, wherein transmission times for the second plurality of bit streams on the plurality of symmetrical data circuit pathways are substantially equal, and wherein *the second multiplexing integrated circuit* receives the forward data clock signal and *symmetrically distributes the forward data clock signal along a plurality of symmetrical clock circuit pathways*, wherein clock transmission times associated with each clock circuit pathway are substantially equal . . . ." (emphasis added).

Figure 11B of Applicant's Specification depicts a demultiplexer circuit in which the circuit pathways, and in particular the clock circuit pathways, are symmetrically patterned to reduce or eliminate the need for delay elements while providing substantially equal transmission times to demultiplexers 482:

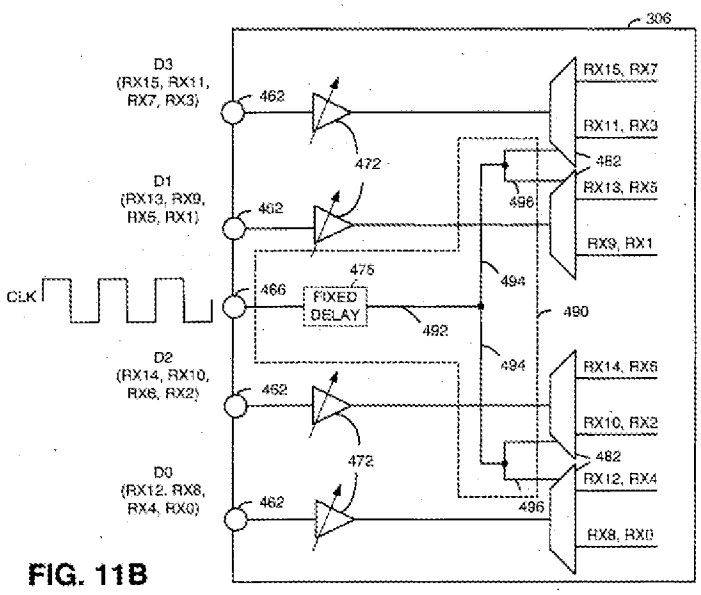

FIG. 11B

As explained in Applicant's Specification at paragraph 0067, "[Figure] 11B illustrates the symmetrical nature of the data clock pathway such that the data clock signal arrives at each demultiplexer 482 at about the same time. This is achieved by having substantially equal

transmission times of the clock signal along the clock distribution circuit. Here, clock distribution circuit 490 comprises a central trunk 492. From this central trunk extend symmetrical branches 494. Depending on the number of multiplexers employed and their physical location, a further set of symmetrical branches 496 may distribute the clock signal to the individual demultiplexers 482. *Central trunk 492 is located approximately midway between the circuit pathways associated with input ports for signals D1 and D2*." (Specification ¶ 0067).

In this regard, Applicant's Independent Claim 26 recites, *inter alia*, a "multistage bit stream demultiplexer, comprising: a *first demultiplexing integrated circuit* that receives a first plurality of bit streams at a first bit rate and that produces a second plurality of bit streams at a second bit rate . . . ; a clock circuit, wherein the clock circuit generates a forward data clock signal; a plurality of *symmetrical data circuit pathways* that transport the second plurality of bit streams from the first demultiplexing integrated circuit; *a second demultiplexing integrated circuit* that receives the second plurality of bit streams from the plurality of symmetrical data pathways, wherein transmission times for the second plurality of bit streams on the plurality of symmetrical data circuit pathways are substantially equal, and wherein the second demultiplexing integrated circuit receives the forward data clock signal and *symmetrically distributes the forward data clock signal along a plurality of symmetrical clock circuit pathways, wherein clock transmission times associated with each clock circuit pathway are substantially equal . . . .*" (emphasis added).

In view of the above, Applicant respectfully submits that each and every element as set forth in Applicant's claimed invention is not found in Chen. Applicant respectfully requests that the rejection to Independent Claims 21 and 26 be withdrawn.

4. Rejection under Section 103

(a) Claims 1, 6, 11 and 12 were rejected under 35 U.S.C. 103(a) as being unpatentable over Chen.

(b) Claims 2, 7-10, 13, 22, 25, 27, and 30 were rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. in view of U.S. Patent No. 6,636,532 to Dorschky ("Dorschky").

(c) Claims 3-5, 14-20, 23, 24, 28, and 29 were rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. in view of Dorschky as applied to claims 2 and 13 above, and further in view of U.S. Published Application 2001/0005158 to Okayasu ("Okayasu").

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the

knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. MPEP § 2142, p. 2100-125 (Rev. 5, August 2006) (citations omitted).

The rejection includes Applicant's Independent Claims 1 and 12. Claims that depend directly or indirectly from these are "construed to incorporate by reference all the limitations of the claim to which [they refer]." 35 U.S.C. § 112, ¶ 4

Akin to the rejection under Section 102 to Applicant's Claims 21 and 26, the Office Action takes Applicant's term "*symmetrically*" and interprets it to fit with Chen's use of the term "synchronous" as used with the synchronous clock 510 shown in Figure 4 of Chen. (Office Action at p. 7). Chen recites that the "synchronous clock 510 . . . synchronizes PHD devices 502-505 and synchronous multiplexer 508." (Chen 6:10-17). Chen, however, is silent with respect to symmetric pathways in which clock transmission times associated with each clock circuit pathway are substantially equal.

Dorschky relates to "correlating phases of a clock signal and data signals to adjust for phase deviations in a network having multiplexers of a first hierarchy concatenated with multiplexers of at least one higher hierarchy." (Dorschky 1:40-43). Dorschky was cited because of "delay means." (Office Action at p. 9). Dorschky recites that its "delay means [are] controlled by the control signals[, which are indicative of phase deviation of the data signals,] to adjust for the phase deviation of the data signals to the clock signal of the higher hierarchy, whereat the delay means at least delay one input signal of each multiplexer of a lower hierarchy." (Dorschky 1:48-52). Dorschky does not, however, recite a clock distribution circuit that includes a plurality of delay elements. Further, Dorschky does not recite symmetrical pathways.

Okayasu relates to a "variable delay circuit, which generates a delay amount." (Okayasu ¶ 0002). Okayasu does not recite a multiplexer, demultiplexer, and/or a high speed bit stream data conversion circuit. Further, Okayasu does not recite symmetrical pathways.

As understood, the reference to "synchronizes" under Chen simply refers to a shared clock, as Chen does not further discuss pathways or layouts of between the devices or the shared

clock. In this regard, Applicant respectfully submits that there is no suggestion or motivation to modify Chen, or for the hypothetical combination of Chen with Dorschky, or Dorschky and Okayasu, to achieve Applicant's claimed invention.

For example, Applicant's Claim 1 recites, *inter alia*, a "high speed bit stream data conversion circuit comprising: . . . *a plurality of symmetrical data circuit pathways* that include pairs of circuit pathways, and that transport the first plurality of bit streams from the first plurality of input ports, and to the plurality of data conversion circuits, . . . ; a clock distribution circuit that receives a data clock signal at a clock port located *at a midpoint of the first plurality of input ports*, and symmetrically distributes the data clock signal to the plurality of data conversion circuits along a plurality of symmetrical clock circuit pathways, wherein the *symmetrical clock circuit pathways* further *include a central trunk coupled to the clock port and wherein the trunk is located between a first pair of circuit pathways*, and *symmetrical pairs of branches that extend from the trunk and couple to the data conversion circuits*, and wherein the clock transmission times associated with each symmetrical clock circuit pathway *are substantially equal*, ..." (emphasis added).

Also, Applicant's Independent Claim 12 recites, *inter alia*, a "method of converting high speed data bit streams from a first bit rate to a second bit rate, wherein the first and second bit rate differ, comprising the steps of: receiving a first plurality of bit streams at a first plurality of input ports; *distributing* the first plurality of bit streams to a plurality of data conversion circuits along a *plurality of symmetrical data circuit pathways*; symmetrically distributing a clock signal to the plurality of data conversion circuits *along a plurality of symmetrical clock circuit pathways*, wherein *clock transmission times associated with each clock circuit pathway are substantially equal*, ..." (emphasis added).

Accordingly, Applicant respectfully submits that a *prima facie* case of obviousness has not been established. There is no suggestion or motivation for the modification of Chen or the hypothetical combination of Chen with Dorschky and/or Okayasu to achieve Applicant's claimed invention of Claim 1 and claims 2-11 that depend directly or indirectly therefrom, of Claim 12 and claims 13-20 that depend directly or indirectly therefrom, of claims 22-25 that depend directly or indirectly from Independent Claim 21, and of claims 27-30 that depend directly or indirectly from Independent Claim 26.

5. Conclusion

As a result of the foregoing, the Applicant respectfully submits that Claims 1-30 in the Application are in condition for allowance, and respectfully requests an early allowance of such Claims.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at ksmith@texaspatents.com.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Garlick Harrison & Markison Deposit Account No. 50-2126.

Respectfully submitted,

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/Kevin L. Smith/
Kevin L. Smith, Reg. No. 38,620
Attorney for Applicant

Garlick Harrison & Markison
P.O. Box 160727
Austin, Texas 78716-0727
(972) 772-8836/office
(972) 772-5033/facsimile